



Circuit Technology

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Millennium Predictions for Printed Circuits

All electronic components must be interconnected and assembled to form a functional and operating system. Electronic packaging is a multidisciplinary technology that combines engineering and manufacturing techniques to convert an electronic circuit into a manufactured assembly.

Since the mid-20th century, the primary element of connecting

components has been the printed wiring board. In order for PWBs to remain so, new construction techniques and advanced materials will be crucial in perfecting a higher density interconnect system.

These improvements are necessary to maximize the benefits of recent advances in semiconductor technology. As computers and modules obtain processing speeds greater than 100 MHz, signal and signal integrity become paramount. With the introduction of the Power PC and Pentium chip products, processing speeds are accelerating on a continuum basis, as can be seen by the high-frequency demands from 1990 to what is projected for the millennium.

Balancing Performance Gains With Cost Increases (1955-1998)
For the past 50 years, printed wiring boards have allowed adjustment to the cost and performance needs of the electronic industry. The first challenge was the double-sided PWB, which was addressed and solved by electroless copper PTH metallization and nickel/gold as an etch-resist metal.

To compensate for embrittlement concerns with soldering to gold, tin/lead high-throw plating solutions were introduced, along with a recyclable alkaline etching solution to reduce waste treatment costs. Perfecting reflow techniques afforded a surface finish that guaranteed solderability—as long as thickness specifications were met, no visible evidence of dewetting occurred and the coating remained bright and shiny.

Processing Speeds, MHz*

	1992	1996	2000
Super computers	200	300	1000
Mainframes	100	200	300
Workstations	50	100	175
Personal computer	20	30	50

As circuit density increased, the need for solder mask posed a problem. The tin/lead melting under the resist could either prevent adhesion or cause the resist to crack, with the potential of entrapping flux residues. Often, post-soldering cleaning was not effective in removing these ionic materials. The potential of current leakage caused by humidity dictated solder mask over bare copper for many applications.

Hot-air solder leveling (HASL) was perfected to meet this requirement. The introduction of surface mount technology in 1982 made SMOBC mandatory for most applications.

Ultra-fine pitch components created a need for planarity and precise volume of solder in each fillet. The meniscus formed when tin/lead solidifies and the thickness variations inherent with this process impose a serious limitation on HASL. Selecting the most reliable, cost-effective surface finish for a particular application now requires a complex evaluation of the advantages/disadvantages of all alternatives.

HDI Requirements

Future needs of the electronic industry predetermine nuances of freedom in properties, such as thermal resistance, ultrathin dielectrics and small hole formation, to provide the foundation

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for MCM-L, PCMIA, smart cards and high-density multilayer technologies.

The cost advantage of organic substrates over ceramic has unveiled avant-garde avenues for PWBs. To respond to this opportunity, improvements in copper foil and laminate technology are pivotal.

Current etching procedures are capable of efficiently providing 125 microns (5 mils) lines/spaces. To conserve real estate, the industry is seeking lines/spaces of 76 microns (3 mils). To accomplish this, a new approach is recommended: Additive/semi-additive technology or fine-line etching of 18 micron ($1/2$ oz) copper foil. These prerequisite extensive learning processes, strict control and increased material cost.

Fine-line etching entails foil fabricated by novel techniques. By adjusting the process of electrodeposition, the grain can be altered from traditional columnar to a fine-grain, non-columnar structure.

Advanced material technology can provide robust solutions from a

variety of polymer and carrier systems that utilize low-thermal-setting polymers (*e.g.*, cyanate ester provides signal transmission speeds of 114 cm/ns to 100 cm/ns of normal FR-4 epoxy materials).

Laminates that assure a lower dielectric constant (D_k) result in benefits of faster conductor speed and thinner interconnects for the same conductor geometries. Those with a lower dissipation factor (D_f) provide improved signal integrity with high frequencies and less signal loss at high frequencies.

Carrier systems of random aramid material have a negative fiber coefficient of thermal expansion and, when combined with advanced resins, have CTEs in the range of 7–9 ppm/°C, compared to standard epoxy glass laminates as high as 16 ppm/°C. This type of material also enables the designer and manufacturer to employ two processes that are incompatible with glass-based substrates: Plasma ablation and laser ablation.

Current Challenges

The decision to place numerous bare die upon a multi-layer, multi-chip substrate presents a dilemma that is being addressed by microvia/buildup methodologies. The goal is to provide construction methods and materials that are cost-effective for producing blind and buried microvias on thin organic substrates. The future of printed circuits depends on the success in developing these advanced construction techniques, as well as improved materials for higher interconnection density. P&SF

**Clyde Coombs, Printed Circuit Handbook, 4th ed., Ch. 9.4, McGraw Hill (1995).*